AMENDMENTS TO THE SPECIFICATION

Please amend the specification as follows:

Replace the paragraph on page 13 beginning on line 11, with the following:

Figures 5 and 6 show an exemplary relationship between the output signal produced at output 900 of the clocked comparator 910 and the voltage on capacitor 510 over time. Figure 5 shows the output signal produced by the clocked comparator when a 100 MHz clock signal is applied to the clock input 940. At a clock frequency of 100 MHz, clock pulses are spaced at an interval of 10 ns. In the example shown, the output of the clocked comparator is high 1160 for one clock pulse (10 ns) and low 1170 for three clock pulses (30 ns). This corresponds to the voltage waveform shown in Figure ~~figure~~ 6. In Figure ~~figure~~ 6, the voltage of the capacitor 510 is shown to begin rising when the output 900 of the clocked comparator goes low (time A), thereby turning on the PMOS transistor 770. The voltage rises for 30 ns, or three clock pulses until time B. At time B, the output of the clocked comparator goes high again, turning off the PMOS transistor. The voltage on the capacitor 510 then begins to drop again while the PMOS device remains off for one clock pulse, or 10 ns (until time C). Accordingly, in the example shown, the duty cycle of the signal output by the clocked comparator 910 is 75% (three on-pulses for every off-pulse).